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DualFALC™

Two-channel E1/T1/J1 Framer and Line Interface Component
PEF 22552
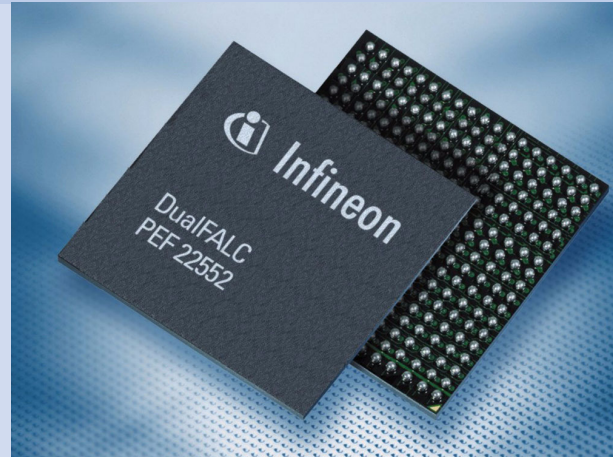
The DualFALC™ is an addition to Infineon's market leading FALC® family of advanced E1/T1/J1 Framer And Line Interface Unit (LIU) components. As a two port E1/T1/J1 framer and line interface unit (LIU), DualFALC is optimized for a range of network equipment including Radio network Controllers, Node B line cards, PBX or SDH/SONET ADMs.

The DualFALC features a unique clock generation unit that accepts any reference clock between 1.02 and 20MHz as well as integrated analog switches for impedance matching or protection switching. Using industry leading DualFALC Evaluation support tools, system developers can shorten design cycles while creating a wide range of highly flexible, low BOM E1/T1/J1 line cards.

Applications

- Wireless base stations
- Router
- Multi-service access platforms,
- Digital loop carriers
- Remote access servers/concentrators
- SONET/SDH Add/Drop multiplexers

Analog Line Interfaces

- Two independent E1/T1/J1 long haul/short haul line interface units
- Software programmable T1/E1/J1
- Integrated analog switches for impedance matching (E1-75/120, T1-100 , J1-110) and protection switching
- Crystal-less wander and jitter attenuation/compensation according to TR 62411 and ETS-TBR 12/13
- Clock generation unit accepts any frequency reference clock from 1.02 MHz to 20 MHz
- Programmable transmit pulse shape for flexible pulse generation
- Receiver sensitivity exceeds -36 dB@772kHz and -43 dB@1024kHz
- Clock signal generation & extraction according to ITU-T G.703 Sec. 13
- Integrated transmit line impedance matching

Frame Aligners

- ITU-T G.704 frame alignment/synthesis for 2.048/1.544 Mbit/s

- Programmable frame formats
  - E1: Double- & CRC Multi-frame
  - T1: F4, F12 (D4), Ext. Super Frame (ESF), F72 (SLC96)
- Detects and generates LOS, AIS and RAI alarms
- CRC-4 performance monitoring
- PRBS generation and monitoring
- Detects & generates LOS, AIS & RAI alarms
- System bus data rate scalable from 1.544 Mbit/s up to 16 Mb/s
- Synchronization Supply Message (SSM) generation and extraction

HDLC Controllers

- 6 HDLC controllers (three per channel) including 128-byte deep FIFO buffers each
- CAS controller with micro-processor or system interface serial access
- Supports signaling system #7
- ANSI T1.403 Bit-Oriented Messages (BOM), generates periodical performance reports

General Features

- Software compatible to Infineon's QuadFALC and OctalFALC
- Intel® or Motorola® type 8/16-bit microprocessor interface
- Serial SPI bus and serial SCI bus slave interfaces
- Low power operation (150mW / channel typical)
- Dual voltage 1.8 V/3.3 V or single voltage 3.3V power supply
- PG-LBGA-160, 15x15mm with 1.0mm ball pitch
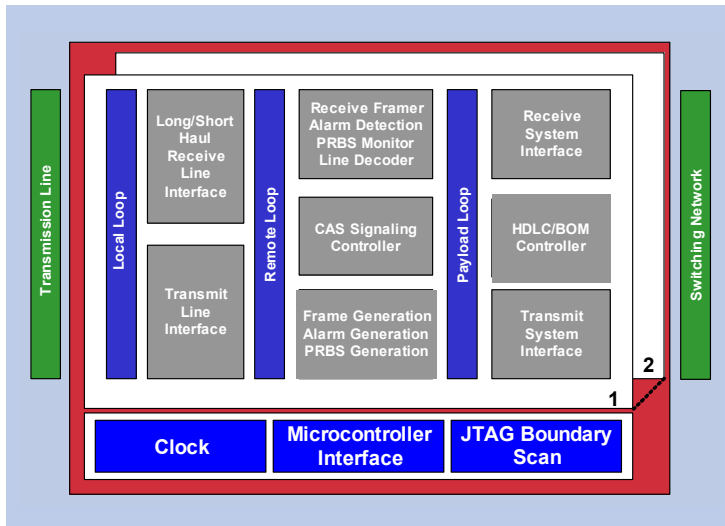- -40degC to +85degC operation
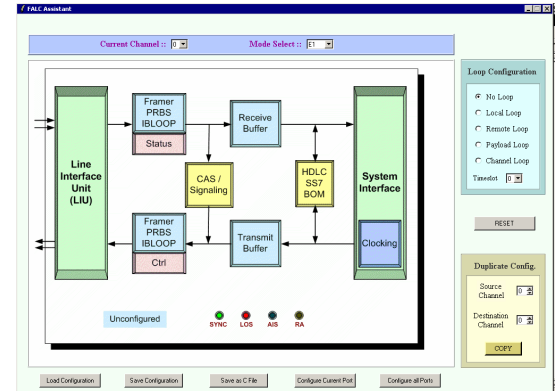- Rohs compliant package

www.infineon.com/falc

Communications

Never stop thinking.

DualFALC PEF 22552 Block Diagram

System Application -
VoIP Primary Access Board

Product Summary

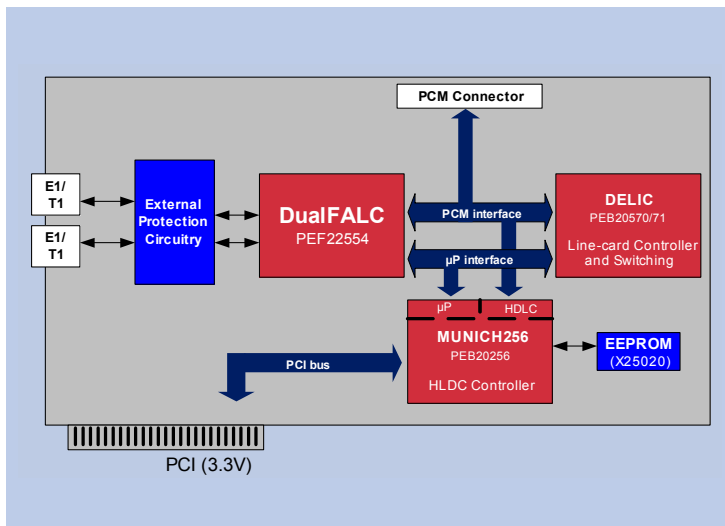| Type	Description	Package
PEF 22552E	DualFALC	PG-LBGA-160

Configuration Assistant Tool

The FALC Configuration Assistant supports the user during design phase.
All DualFALC functional blocks can be configured by a GUI supporting the low level API driver.

Documentation and Support Package

- Data Sheet
- Application Notes
- Hardware Evaluation System EASY 22552 with Schematics and Layout information
- WinEASY Software for MS Windows 98SE/NT/2000/XP CD-ROM Support Package
- Support Software (portable low level API driver)
- Configuration Assistant for rapid porting of device configuration to customer designs.
- Analog front end calculator
- Flexible master clocking calculator

Published by Infineon Technologies AG